**Computer Architecture (2)**

**Rubric - Project Final Submission (Functionality)**

Please fill in the 2nd column of the following table:

|  |  |
| --- | --- |
| Project title | Hash Functions Sha256 pipeline |
| Group Members | 1-motasem rafati  2-ahmad Alzoul  3- |
| Total number of Pipeline Stages | 6 stages |
| Correctness of the design checked (compared to a software implementation)? Yes/No | yes |
| Design is implemented in Verilog? Fully/Partially | yes but only miss the padding part |
| Simulations show:  1-only partial results of stages  2- only final results  3- Both partial and final results | Both partial and final results |
| Simulations show cycle by cycle results? Yes/No | yes |
| Number of simulated clock cycles? | 64 cc |
| Design is compared (analytically/experimentally) with single-cycle implementation? Yes/No | analytically .no many cycles |